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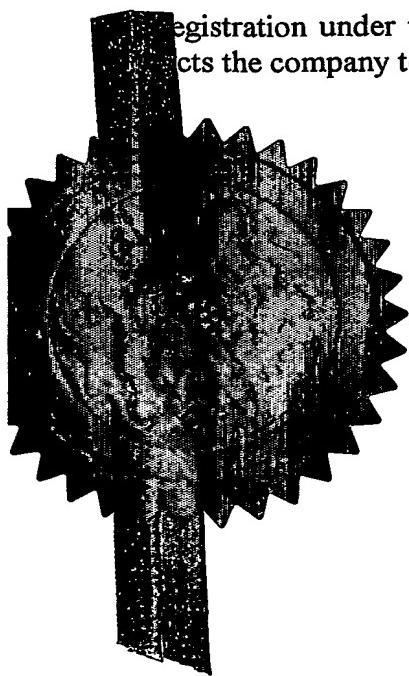
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GB 0325584.1

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ELONICS LIMITED,  
5 Craiglockhart View,  
EDINBURGH,  
EH14 1BX,  
United Kingdom

Incorporated in the United Kingdom,

[ADP No. 08924649001]

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1/77

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2. Patent application number

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- 3 NOV 2003

3. Full name, address and postcode of the or of each applicant (*underline all surnames*)

David Srodzinski  
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ACI APPLICATION FILED 31/8/04

Patents ADP number (*if you know it*)

7966252001

If the applicant is a corporate body, give the country/state of its incorporation

4. Title of the invention

Method and apparatus for adapting an information carrying signal

5. Name of your agent (*if you have one*)

"Address for service" in the United Kingdom to which all correspondence should be sent  
*(including the postcode)*

Kennedys Patent Agency Limited  
Floor 5, Queens House  
29 St Vincent Place  
Glasgow  
G1 2DT

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0805 824 0002

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8. Is a Patents Form 7/77 (Statement of inventorship and of right to grant of a patent) required in support of this request?

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- 9. Accompanying documents:** A patent application must include a description of the invention. Not counting duplicates, please enter the number of pages of each item accompanying this form:

Continuation sheets of this form 30

Description *D*

Claim(s)

Abstract

Drawing(s) *9 ONLY*

- 10. If you are also filing any of the following, state how many against each item.**

**Priority documents****Translations of priority documents**

**Statement of inventorship and right to grant of a patent (Patents Form 7/77)**

**Request for a preliminary examination and search (Patents Form 9/77)**

**Request for a substantive examination (Patents Form 10/77)**

**Any other documents (please specify)**

- 11. I/We request the grant of a patent on the basis of this application.**

Signature(s)

*Kennedy*

**KENNEDYS PATENT AGENCY LTD Date 30.10.03**

- 12. Name, daytime telephone number and e-mail address, if any, of person to contact in the United Kingdom**

David Fulton

Tel: 0141 226 6826

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1    Method And Apparatus For Adapting An Information Carrying  
2    Signal

3

4    This invention relates to the field of communications  
5    systems. More particularly, this invention relates to a  
6    method and apparatus for adapting an information carrying  
7    signal. The method and apparatus can be readily employed  
8    within a transmitter of a communication system so as to  
9    overcome signal impairment effects within the system.  
10   The invention has particular use as an equalisation  
11   element in the field of fibre optic communications  
12   networks to counteract dispersion and other complex  
13   signal impairments.

14

15

16    Background Art

17

18    Electronically adjustable equalization transmitter  
19    schemes for communications systems are well known in the  
20    art. Such a scheme is embodied in US Patent No. US  
21    6,393,062 entitled "Methods and circuits for generating a  
22    pre-emphasis waveform". This scheme relies on pre-  
23    compensating a waveform by selectively boosting the  
24    electronic signal to a value larger than the nominal

1 signal, essentially providing data-dependant pulse  
2 amplitude modulation.

3

4 There are however several major drawbacks with this  
5 scheme. In the first instance pulse amplitude modulation  
6 is not a suitable control method for increasing the  
7 optical intensity in order to provide compensation in an  
8 optical fibre system because:

9 a) in standard systems amplitude information is  
10 removed using a pre-laser limiting or clipping  
11 function in order to simplify driver electronics;  
12 and

13 b) lasers are very non-linear devices and so  
14 amplitude modulation is non-linearly related to  
15 optical intensity.

16

17 As a result lasers do not respond or do not respond well  
18 to pulse amplitude modulation.

19

20 Secondly, with higher data-rate signals, for example  
21 greater than 10 Gbps, such a scheme is very difficult to  
22 practically implement in a low cost electronic CMOS or  
23 BiCMOS silicon technologies as the required switching  
24 speeds and slew rates will be unwieldy and difficult to  
25 control accurately.

26

27 A further drawback is that the amplitude and settling  
28 characteristics relied upon to perform the equalisation  
29 are subject to unacceptable variations and so are not  
30 suitable for precision or high speed applications. As  
31 shown in a particular embodiment, the scheme requires  
32 additional circuitry to accurately control the amount of  
33 boost which in-turn increases complexity, power and cost  
34 of the system.

1  
2 Furthermore, the signal boosting scheme described  
3 requires the driving of a larger than normal signal.  
4 This may not always be possible given power supply  
5 constraints or, conversely, requires some signal  
6 amplitudes to be reduced, which does not maximise  
7 available signal to noise available for these signals.

8  
9 European Patent Application No. EP 0,884,867 describes a  
10 system for "Equalization, pulse shaping and regeneration  
11 of optical signals". In particular this document teaches  
12 of an equalisation arrangement for use in optical systems  
13 with optical fibre media. The scheme relies on  
14 equalisation using weighted tap filter crafted that  
15 employs optical components in the optical domain. Such  
16 an approach again exhibits several issues inherent  
17 disadvantages.

18  
19 Firstly, such equalisation can only compensate for linear  
20 effects that contribute to Inter-Symbol-Interference  
21 (ISI) such as those caused by dispersion. However, other  
22 non-linear effects including laser and fibre chirp,  
23 changes in fibre characteristics with optical intensity,  
24 duty cycle distortions and unequal rise/fall times of the  
25 transmitter or receiver are not addressed.

26  
27 Secondly, the system is relatively expensive to make as  
28 it relies on several expensive optical amplifiers,  
29 optical monitors and customised and precise lengths of  
30 delay matched optical fibres.

31  
32 Thirdly, the physical size and inherent power  
33 requirements make such schemes less desirable or  
34 practical in modern installations.

1  
2 It is an object of an aspect of the present invention to  
3 provide a method and apparatus for filtering an  
4 information carrying signal. In particular this method  
5 and apparatus can be employed for equalisation of the  
6 information carrying signal so as to overcome the  
7 problematic features of the prior art.  
8  
9

10 Statements of Invention

11

12 According to a first aspect of the present invention  
13 there is provided a method of adapting an information  
14 carrying signal that comprises a plurality of data pulses  
15 that exhibit a range of pulsewidths and which are  
16 generated by a transmitter for transmission through a  
17 propagation medium, the method comprising the step of  
18 introducing one or more sub-pulses to one or more of the  
19 plurality of data pulses prior to the information  
20 carrying signal entering the signal propagation medium  
21 wherein a pulsewidth of each of the one or more sub-  
22 pulses is less than a minimum pulsewidth of the plurality  
23 of data pulses.

24

25 According to a second aspect of the present invention  
26 there is provided a method of adapting an information  
27 carrying signal that comprises a plurality of data pulses  
28 that exhibit a range of pulsewidths and which are  
29 generated by a transmitter for transmission through a  
30 propagation medium, the method comprising the step of  
31 altering one or more edges of one or more of the  
32 plurality of data pulses prior to the information  
33 carrying signal entering the signal propagation medium.

34

1 According to a third aspect of the present invention  
2 there is provided a method of adapting an information  
3 carrying signal that comprises a plurality of data pulses  
4 that exhibit a range of pulsewidths and which are  
5 generated by a transmitter for transmission through a  
6 propagation medium, the method comprising the steps of:

7

- 8       1) introducing one or more sub-pulses to one or more  
9       of the plurality of data pulses prior to the  
10      information carrying signal entering the signal  
11      propagation medium wherein a pulsewidth of each of  
12      the one or more sub-pulses is less than a minimum  
13      pulsewidth of the plurality of data pulses; and  
14       2) altering one or more edges of one or more of the  
15      plurality of data pulses prior to the information  
16      carrying signal entering the signal propagation  
17      medium.

18

19 Preferably, the one or more sub-pulses are introduced to  
20 one or more of the plurality of data pulses when the data  
21 pulse exhibits a pulsewidth above a first predetermined  
22 pulsewidth of the plurality of data pulses so as to  
23 provide a method for low frequency filtering the  
24 information carrying signal.

25

26 Alternatively, the one or more sub-pulses are introduced  
27 to one or more of the plurality of data pulses when the  
28 data pulse exhibits a pulsewidth below a second  
29 predetermined pulsewidth of the plurality of data pulses  
30 so as to provide a method for high frequency filtering  
31 the information carrying signal.

32

33 Preferably, the one or more edges of one or more of the  
34 plurality of data pulses are altered when the data pulse

- 1 exhibits a pulsewidth above a third predetermined  
2 pulsewidth of the plurality of data pulses so as to  
3 provide a method for low frequency filtering the  
4 information carrying signal.
- 5
- 6 Alternatively, the one or more edges of the one or more  
7 of the plurality of data pulses are altered when the data  
8 pulse exhibits a pulsewidth below a fourth predetermined  
9 pulsewidth of the plurality of data pulses so as to  
10 provide a method for high frequency filtering the  
11 information carrying signal.
- 12
- 13 Most preferably the first and/or the third predetermined  
14 pulsewidths of the plurality of data pulses corresponds  
15 to the minimum pulsewidth of the plurality of data pulses  
16 so as to provide a method of equalising the information  
17 carrying signal.
- 18
- 19 Most preferably an amplitude of the one or more sub-  
20 pulses is of an opposite sign to an amplitude of an  
21 associated data pulse.
- 22
- 23 Preferably the timing of introducing the one or more sub-  
24 pulses to one or more of the plurality of data pulses is  
25 variable.
- 26
- 27 Most preferably, the number of sub-pulses introduced is  
28 directly dependent upon the pulsewidth of the associated  
29 data pulse. Alternatively, the pulsewidth of the one  
30 sub-pulse is directly dependent upon the pulsewidth of  
31 the associated data pulse.
- 32

1 Preferably the one or more edges of the one or more data  
2 pulses is altered by time shifting a rising and/or a  
3 falling edge of an associated data pulse.

4

5 Optionally the time shifting of the rising and/or the  
6 falling edge of the associated data pulse is by a  
7 predetermined value. Alternatively, the time shifting of  
8 the rising and/or the falling edge of the associated data  
9 pulse is directly dependent upon the pulselength of the  
10 associated data pulse.

11

12 Preferably the time shifting of the rising edge of an  
13 associated data pulse comprises advancing in time the  
14 rising edge.

15

16 Preferably the time shifting of the falling edge of an  
17 associated data pulse comprises delaying in time the  
18 falling edge.

19

20 According to a fourth aspect of the present invention  
21 there is provided an electronic circuit suitable for  
22 adapting an electronic input signal of a transmitter, the  
23 electronic input signal comprising a plurality of  
24 electrical data pulses, the electronic circuit comprises  
25 an electronic input channel, a clock pulse phase delay  
26 circuit, a signal processor and an electronic output  
27 channel wherein the signal processor analyses one or more  
28 of the plurality of electrical data pulses supplied on  
29 the electronic input channel and one or more clock pulse  
30 phase delay signals provided by the clock pulse phase  
31 delay circuit so as to introduce one or more electronic  
32 sub-pulse to one or more of the plurality of electrical  
33 data pulses so as to provide an adapted electronic output  
34 signal on the electronic output channel.

1  
2 According to a fifth aspect of the present invention  
3 there is provided an electronic circuit suitable for  
4 adapting an electronic input signal of a transmitter, the  
5 electronic input signal comprising a plurality of  
6 electrical data pulses, the electronic circuit comprises  
7 an electronic input channel, a clock pulse phase delay  
8 circuit, a signal processor and an electronic output  
9 channel wherein the signal processor analyses one or more  
10 of the plurality of electrical data pulses supplied on  
11 the electronic input channel and one or more clock pulse  
12 phase delay signals provided by the clock pulse phase  
13 delay circuit so as to alter one or more edges of one or  
14 more of the plurality of electrical data pulses so as to  
15 provide an adapted electronic output signal on the  
16 electronic output channel.

17  
18 According to a sixth aspect of the present invention  
19 there is provided an electronic circuit suitable for  
20 adapting an electronic input signal of a transmitter, the  
21 electronic input signal comprising a plurality of  
22 electrical data pulses, the electronic circuit comprises  
23 an electronic input channel, a clock pulse phase delay  
24 circuit, a signal processor and an electronic output  
25 channel wherein the signal processor analyses one or more  
26 of the plurality of electrical data pulses supplied on  
27 the electronic input channel and one or more clock pulse  
28 phase delay signals, provided by the clock pulse phase  
29 delay circuit so as to introduce one or more electronic  
30 sub-pulse to one or more of the plurality of electrical  
31 data pulses and to alter one or more edges of one or more  
32 of the plurality of electrical data pulses so as to  
33 provide an adapted electronic output signal on the  
34 electronic output channel.

1  
2 Most preferably the clock pulse phase delay circuit  
3 comprises means for supply a first clock pulse and one or  
4 more phase delayed clock pulses to the signal processor.  
5

6 Preferably the signal processor comprises first  
7 electronic means for producing an internal signal pulse  
8 when subsequent electrical data pulses exhibit  
9 substantially the same value.

10  
11 Preferably the signal processor further comprises a  
12 second electronic means for introducing an electronic  
13 sub-pulse to the electronic input signal when the  
14 internal signal pulse is detected by the second  
15 electronic means.

16  
17 Preferably the signal processor further comprises a third  
18 electronic means for altering in time the rising or  
19 falling edge of an electrical data pulses.

20  
21 Most preferably the timing of the first electronic means  
22 is controlled by the first clock pulse.  
23

24 Preferably the second and third electronic means are  
25 controlled by the combination of the first clock pulse  
26 and the one or more phase delayed clock pulses.  
27

28  
29 Brief Description of Drawings  
30

31 In the following detailed description of the preferred  
32 embodiments or mode, reference is made to the  
33 accompanying drawings, which form part hereof, and in  
34 which are shown, by way of illustration, specific

1 embodiments in which the invention may be practised. It  
2 is to be understood that other embodiments may be  
3 utilised and structural changes may be made without  
4 departing from the scope of the present invention.

5

J:

6 FIGURE 1 shows a system block diagram of a typical  
7 communication channel that will be used for reference  
8 purposes;

9

10 FIGURE 2 shows a system block diagram of a typical long-  
11 haul fibre optic communication channel that incorporates  
12 an adaptable signal processing element, shown within the  
13 transmitter function, in accordance with an aspect of the  
14 present invention;

15

16 FIGURE 3 shows an example of a standard transmitted (in)  
17 and received (out) signal waveform before any wave signal  
18 processing in the transmitter is applied;

19

20 FIGURE 4 shows the resulting "eye diagram" of the  
21 information presented in Figure 3;

22

23 FIGURE 5 shows details of the operation of the adaptable  
24 signal processing element employed to equalise the  
25 received (out) signal waveform at the output of the  
26 transmitter and in particular schematically presents  
27 definitions of coefficient terms employed for achieving  
28 this result.

29

30 FIGURE 6 shows an example of a modified transmitted (in)  
31 and received (out) signal waveform after the adaptable  
32 signal processing element within the transmitter is  
33 applied;

34

1 FIGURE 7 shows the resulting improved "eye diagram" of  
2 the information presented in Figure 6;

3

4 FIGURE 8 shows a top level schematic view of the  
5 preferred embodiment of the adaptable signal processing  
6 element;.

7

8 FIGURE 9 shows detail of the clock pulse signal waveforms  
9 employed within the adaptable signal processing element  
10 such that it operates to equalise the received (out)  
11 signal waveform;

12

13 FIGURE 10 shows schematic detail of the signal processor  
14 apparatus; and

15

16 FIGURE 11 shows details of the waveforms generated within  
17 adaptable signal processing element of Figure 5.

18

19

20 Detailed Description

21

22 Adaptable schemes can be used in order to improve some  
23 desired metric of a communications system's performance.  
24 By improving the system performance an adaptable system  
25 allows higher bandwidth or higher data-rate or longer  
26 reach or more compact or less expensive systems to be  
27 made.

28

29 A detailed description of the method ad apparatus for  
30 such an adaptable system shall now be described and in  
31 particular to its employment as an equaliser for an  
32 information carrying signal transmitted within an optical  
33 system. This equalisation can be used to counteract

bandwidth limiting or other signal impairments within the channel].

3

4 Within a communications system typical signal impairment  
5 or degradation mechanisms include the rise time, fall  
6 time, bandwidth or other distortion of the receiver or  
7 transmitter, dispersion, chirp, reflection and bandwidth  
8 limitations within the media and interference from other  
9 signals. The words signal impairments or degradation  
10 mechanism will be used extensively throughout this  
11 document for any linear or non-linear, stationary or non-  
12 stationary or other non-ideal affect anywhere in the  
13 communications channel that causes the received signal to  
14 be adversely affected.

15

16 The resultant effects of these degradation mechanisms on  
17 the signal are often dependant on the inter-relationship  
18 of the signal being transmitted and the degradation  
19 mechanism itself. Within some bounds these are  
20 repeatable effects. These will be generally referred to  
21 as deterministic effects throughout this document.

22

23 The task of equalisation or compensation is to modify the  
24 physical characteristics of an information carrying  
25 signal in order to correct, accommodate or rectify some  
26 impairment in it. In an aspect of the present invention  
27 the equalisation is achieved by synthesising a new  
28 transmitted wave-shape using a high speed signal  
29 processor. This signal processing, synthesis and  
30 resultant equalisation is achieved using a technique  
31 whereby energy is added or subtracted to the wave shape  
32 in the form of constructive or destructive sub-pulses  
33 and/or by manipulating within the information carrying  
34 signal individual pulse edge positions. The method and

1 apparatus for the preferred embodiment of this are as  
2 follows.

3

4 A typical one-way communications system is shown in  
5 Figure 1. The channel 6 transmits its input signal, in  
6 1, via the transmitter 2, through the media 3, to the  
7 receiver 4 and out in the form of output signal 5.

8

9 A typical long-haul fibre optic communication showing the  
10 preferred embodiment is shown in Figure 2. The  
11 transmitter 2 includes the adaptable signal processor 7  
12 that provides for wave synthesis equalisation in front of  
13 the optical source 8. The input signal 1, is modified by  
14 the action of the adaptable signal processor to produce  
15 the equalised electronic signal, ewave 25. The optical  
16 source converts the electronic signal into an equivalent  
17 optical signal, owave 26. The media 3, here an optical  
18 fibre, itself is shown partitioned into smaller lengths  
19 with optical amplifiers 11 used to boost the signal along  
20 the length, as is typical of these systems, in order to  
21 maximise transmission distances. Amplifiers or repeaters  
22 11 are optionally required as the signal 1 becomes  
23 attenuated with distance due to losses within the optical  
24 fibre 3. The optical signal 26 is received at the  
25 optical detector 9 and amplified to an electrical signal  
26 by the post amp 10.

27

28 Figure 3 shows the time-domain input and output waveforms  
29 of the entire communications system represented in Figure  
30 2 when the signal processing element 7 is disabled. The  
31 figure shows the input signal waveform 1 and the modestly  
32 distorted output signal waveform 5 when no equalisation  
33 or other correction is employed. Note that the exact  
34 output waveform 5 is for illustrative purposes only and

1 more or less complex distortion can occur, and for this  
2 purpose no random or further deterministic jitter is  
3 shown. The waveforms drawn illustrate a non return to  
4 zero (NRZ) signalling scheme which is most likely  
5 implemented as a differential signal with the signal  
6 swinging above (positive) and below (negative) the zero  
7 axis. Where the signal is intended to be digital or  
8 binary in nature the signals may be alternatively  
9 represented by digital signals where a logical "one" is a  
10 differentially positive signal and a logical "zero" is a  
11 differentially negative signal.

12

13 Figure 4 shows an alternative and readily used time-  
14 domain representation of the output waveform 5 as  
15 described in Figure 3 and called an "eye-diagram". The  
16 purpose of the post receiving stage (not shown) is to  
17 determine the optimal sampling point, for example in the  
18 middle of the "eye" 14 and decide whether a "one" or a  
19 "zero" was sent. However making a decision on whether  
20 the signal should be a "one" or a "zero" is made more  
21 difficult by the data jitter 15 and eye closure 16. The  
22 jitter 15 increases and the eye closes 16 due to a number  
23 of impairment and degradation mechanisms. This commonly  
24 manifests itself as inter-symbol interference as  
25 neighbouring bit-patterns constructively or destructively  
26 interfere.

27

28 Figure 5 shows a definition of a new input waveform  
29 "wave", synthesised using the adaptable signal processor  
30 7. The top waveform 25 drawn illustrates the electrical  
31 signal, ewave 25, using a NRZ signalling scheme which is  
32 most likely implemented as a differential signal with the  
33 signal swinging above (+ve) and below (-ve) the zero  
34 axis.

1  
2 Where the signal is intended to be digital or binary in  
3 nature the signals may be alternatively represented by  
4 digital signals where a logical "one" is a differentially  
5 positive signal and a logical "zero" is a differentially  
6 negative signal.

7  
8 The lower waveform in Figure 5 represents the resultant  
9 optical output, owave 26, generated by the optical source  
10 8. This waveform illustrates that the light is either on  
11 or off as controlled by the electronic signal ewave 25.  
12 Therefore, an important advantage of this scheme is  
13 clearly visible in that this scheme does not at all rely  
14 on any amplitude characteristic of the electronic signal  
15 ewave 25 or intensity response from the optical source 8  
16 to an electronic amplitude in order to achieve  
17 equalisation. This is important as the optical source  
18 driving electronics normally would contain a limiting  
19 amplifier and the optical source would be driven into a  
20 power maximum condition, rather than linearly controlled,  
21 as the source is extremely non-linear in nature.

22  
23 Electronic signal ewave 25 shows all rising edges 19, or  
24 all falling edges 20 can be independently extended or  
25 reduced in time, of dTf 21 or dTr 22 respectively, in  
26 order to alter the spatial zero crossing and adding or  
27 reducing energy within the transmitted bit patterns. This  
28 can counter-act artefacts including edge distortion, non-  
29 linear rise fall times, duty cycle distortions and laser  
30 chirp.

31  
32 In addition energy can be added to a transmitted "zero"  
33 by temporarily inverting the optical signal 30 so as to  
34 insert a short pulse of "one" 17, with duration dTl 23,

1 and energy can be independently removed from a  
2 transmitted "one" by temporarily inverting the optical  
3 signal 30 so as to inserting a small pulse of "zero" 18,  
4 with duration dTh 24. This is a remedy for equalising  
5 modal, chromatic and polarisation distortion within the  
6 optical fibre or other bandwidth limitations. In so  
7 doing the adaptable signal processor 7 stops symbol  
8 dependant energy over-spill from one symbol to the next  
9 and minimises interference between symbols and removes  
10 ISI. The input waveform 1 is thus pre-distorted by the  
11 adaptable signal processor 7. This technique is most  
12 appropriate to optical systems because the optical source  
13 either usually incorporates a limiter function in the  
14 optical pre-drive circuitry or the optical source 8 is  
15 operated at near maximum photonic energy output or is so  
16 non-linearly compressed so as to act like a limiting  
17 function. It is therefore only the existence of the  
18 electronic signal ewave 25 above or below the zero-cross  
19 discrimination point and not the signal amplitude that  
20 warrants attention and suitably exploited when  
21 synthesising this equaliser.

22

23 Figure 6 shows the time-domain input and output waveforms  
24 in a communications system employing this invention. The  
25 figure shows the synthesised electronic signal ewave 25  
26 and the now less distorted output signal 5 after  
27 equalisation has been employed. Note this waveform 25 is  
28 for illustrative purposes only and no random jitter is  
29 shown and depending on the compensating parameters set  
30 the waveform can be more or less equalised.

31

32 Figure 7 shows the resulting improved "eye diagram" of  
33 the information presented in Figure 6. The job of the  
34 receiver 4 is made far easier because the data jitter 15

1 (normally measured in ps) and the eye closure 16  
2 (normally measured in dBs) are greatly improved over that  
3 presented in Figure 4. Hence the sampling point 14 is  
4 more easily obtained and tracked than that shown in  
5 Figure 4.

6

7 Figure 8 shows a preferred embodiment of a circuit  
8 schematic of the adaptable signal processor 7. It can be  
9 seen to comprise the input signal, in 1, and its  
10 synchronous clock "clk" signal 51 which are employed to  
11 produce output "ewave" signal 25 from a signal processor  
12 65. The apparatus shows four programmable time delay  
13 circuits dt1 52, dt2 54, dt3 56 and dt4 58. The time  
14 delay circuits produce four phases of "clk" 51, "clkp1"  
15 53, "clkp2" 54, "clkp3" 57 and "clkp4" 59 that are  
16 delayed but synchronous versions of "clk" 51. The time  
17 delay circuits are independently controlled by  
18 coefficient words Cp1 60, Cp2 61, Cp3 62 and Cp4 63. The  
19 coefficient words are stored in a register bank 64 that  
20 can be updated and refreshed as appropriate by a micro  
21 controller or such scheme. The time delay circuits 52,  
22 54, 56 and 58 can be readily implemented using, for  
23 example, unit delay cells, phase interpolation or delay  
24 locked loop techniques or any other scheme that allows a  
25 signal to be controllably delayed.

26

27 Figure 9 shows a particular electronic waveform 25  
28 generated by the adaptable signal processor 7 when  
29 employed in its preferred embodiment as an equalising  
30 element. Figure 9 further comprises schematic  
31 representations of the "clk" signal 51 and the four  
32 generated phases "clkp1" 53, "clkp2" 55, "clkp3" 57 and  
33 "clkp4" 59. It should be noted that the clocks shown are  
34 all shown at full rate, however similar schemes could be

1 derived using sub-rate clocks without departing from the  
2 scope of this invention.

3

4 In particular:

- 5 • "clkp1" 53 rising marks the falling edge 20 of the  
6 "ewave" signal 25, and can be positioned to rise  
7 before or after the edge of the "clk" 51 signal  
8 thus supporting pre-emption or postponing of the  
9 falling edge 20;
- 10 • "clkp2" 55 rising marks the rising edge 19 of the  
11 "ewave" signal 25, and can be positioned to rise  
12 before or after the rising edge of the "clk" 51  
13 signal thus supporting pre-emption or postponing  
14 of the rising edge 19;
- 15 • "clkp3" 57 marks the leading edge of the inversion  
16 sub pulses 17 and 18 of the "ewave" signal 25; and
- 17 • "clkp4" 59 marks the trailing edge of the  
18 inversion sub pulses 17 and 18 of the "ewave"  
19 signal 25.

20

21 As the inversion pulses 17 and 18 are broadened by the  
22 action of the clocks so more energy is added or removed  
23 from the information carrying signal generated by the  
24 optical source 8. A second process for varying the  
25 energy within the information carrying signal is achieved  
26 by shifting in time the inversion sub pulses 18 and 19  
27 through the controlled operation of the clocks. These  
28 sub pulses can either be shifted in time towards a rising  
29 edge 19 or towards a falling edge 20 so that energy can  
30 be accurately removed or added to these edges as  
31 appropriate.

32

33 In a preferred embodiment the +ve sub pulse inversion 17  
34 and the -ve sub pulse inversion 18 are delimited by the

1 same timing clock edges, namely "clkp3" 57 and "clp4" 59.  
2 It will be appreciated by one skilled in the art that  
3 this need not necessarily be the case and in other  
4 embodiments, the +ve and -ve inversion sub pulses, 17 and  
5 18, could be readily made independently controllable.  
6 This could be achieved via the incorporation of  
7 additional time delay elements so as to generate  
8 additional clocks and appropriate changes to the signal  
9 processor 65 in order to include this data dependency.

10

11 Further detail of the signal processing block 65 is  
12 presented in Figure 10. In summary:

- 13     • Elements "inv" 114, 116, 110 act to logically  
14         invert the signal between their input and their  
15         output values;
- 16     • Elements "buf" 115, 109 act to buffer the signal  
17         between their input and their outputs, often used  
18         as unit delay elements to match "inv" elements for  
19         timing purposes;
- 20     • Element "xor" 113 act to logically convert the  
21         signal between their input and their outputs, such  
22         that the output is only a logic high when one and  
23         only one input is logically high;
- 24     • Elements "and" 107, 111, 112 act to logically  
25         convert the signal between their input and their  
26         outputs, such that the output is only a logic high  
27         when both inputs are logically high; and
- 28     • Elements "latch" 100,101,102,103,104,105,106 act  
29         to logically convert the signal between their  
30         input and their outputs, such that the output is a  
31         copy of its input but delayed one clock cycle by  
32         the action of the respective clk so as to act as a  
33         memory element that latches its input to its  
34         output.

1  
2 It will again be apparent to those skilled in the art  
3 that other elemental logical functions can be used to  
4 form equivalent logical functions within Figure 10  
5 without departing from the scope of this invention. It  
6 should also be noted that latch elements 100, 103 and 105  
7 are optional elements, and are incorporated for timing  
8 synchronisation purposes only.

9

10 The purpose of the logic elements indicated as Arm A 130  
11 is to produce a "pulse" signal 121. Figure 10 shows that  
12 the input signals to Arm A comprise the input signal "in"  
13 1 and the clock signal "clk" 51. A next sample output  
14 S(n) 122, a present sample output S(n+1) 123 and a  
15 previous sample output S(n+2) 124 are the outputs from  
16 the latches 100, 101 and 102, respectively in response to  
17 clock signal "clk" 51. The internal "pulse" signal 121  
18 is thus generated whenever two identical consecutive pre-  
19 ceding bits in S(n+1) 123 and S(n+2) 124 are detected,  
20 shown here generated by the "xor" function of element 113  
21 and inversion in "inv" 114 in order to produce the  
22 correct pulse signal 121.

23

24 The purpose of Arm C 132 is to produce a pulse'' signal  
25 129 so providing a means for generating sub pulses 17 and  
26 18. Arm C 132 comprises elements 109 "buf" employed to  
27 provide a delay element to match that introduced by  
28 element "inv" 110. Element 111 "and" acts so as to  
29 create a shortened gating pulse pulse' 128 as defined by  
30 the edges of "clkp3" 57 and "clkp4" 59, and the  
31 coincidence of their high periods. The shortened pulse  
32 pulse'' 129 is then produced from the output of element  
33 "and" 112 under the gating control of the internal pulse  
34 121 employed here as a control signal. The pulse'' 129

1 gating signal is therefore data dependant, as determined  
2 by Arm A 130, and thus the sub pulse are data dependently  
3 controlled so as to either allow normal 17 or inverted 18  
4 sub pulses to be multiplexed by "mux" 108 onto on the  
5 electronic signal ewave 25. In so doing bit symbols can  
6 be temporarily inverted and electronic equalisation  
7 provided without any requirement for normal amplitude  
8 modulation techniques being employed to the optical  
9 signal 30.

10

11 The purpose of Arm B 131 is to produce an  $S(n+1)''$   
12 signal 127 and so provide a means so varying the rising  
13 and falling edges 20. Arm B 131 comprises latch  
14 elements 104 and 106 that act to transfer the data from  
15 the controlled phase delayed clock signals "clkp1" 53 and  
16 "clkp2" 55 respectively in order to advance or retard the  
17 timing edges in the signals  $S(n+1)'$  125 and  $S(n+1)''$  126.  
18 Logical "and" element 107 provides the logical function  
19 to produce the new signal  $S(n+1)''$  127, which contains  
20 identical data to  $S(n+1)$  123 except that its rising and  
21 falling edges have been manipulated by the action of  
22 "clkp1" 53 and "clkp2" 55. Element 116 "inv" provides a  
23 logical inversion and element 115 "buf" provides a time  
24 delay buffer to match the delay introduced by "inv" of  
25 116. Subsequent modification is done by "Mux" 108 which  
26 outputs electronic signal ewave 25 as either normal or  
27 inverted copies of the signal  $S(n+1)''$  under control of  
28 the pulse" 129 signal.

29

30 The synthesised input electronic signal ewave 25 is shown  
31 in Figure 5 showing rising edges 19, or falling edges 20  
32 that can be extended or reduced in time, of dTf 21 or dTr  
33 22 respectively, and energy removed from a "zero" by a  
34 short pulse of "one" 17, with duration dTl 23, and energy

1 removed from a "one" by inserting a small pulse of "zero"  
2 18, with duration dTh 24. However in alternative  
3 embodiments not all features of the method are required  
4 to be employed such that the edge time extension or  
5 reduction effects and/or the sub pulse insertion effects  
6 can be used to lesser degree, or completely removed. An  
7 associated reduction in the required apparatus to  
8 implement these solutions would then occur. Particular  
9 alternative embodiments can be achieved by:

10

- 11 1) Excluding Arm B 131 so that no edge modifications  
12 are possible. In this embodiment the signal  
13 S(n+1)''' 127 would be provided directly by the  
14 S(n+1) 123 signal;
- 15 2) Excluding within Arm B 131 elements 103 and 104,  
16 that control the rising edge of electronic signal  
17 ewave 25, or 105 and 106, that control the falling  
18 edge of electronic signal ewave 25. In this  
19 embodiment only rising or falling edge  
20 modifications respectively are possible and  
21 requires the signal S(n+1)' 125 or S(n+1)'' 126 to  
22 be replaced by S(n+1) 123, as appropriate;
- 23 3) Excluding within Arm C "clkp3" 57 and "buf" 109  
24 and replacing with "clk" 51 so that the rising  
25 edge of pulse" 129 is determined directly by  
26 "clk" 51 and is not controllable.
- 27 4) Excluding within Arm C "clkp4" 59 and "inv" 110  
28 and replacing with "clk" 51 so that the falling  
29 edge of pulse" 129 is determined directly by  
30 "clk" 51 and is not controllable.

31

- 32 In a further alternative embodiment the width of the sub  
33 pulses 17 and 18 widths can be applied independently to  
34 either the high or low signals within the data sequence.

1 This is achieved by replacing the "xor" 113 with parallel  
 2 "and" and "nand" functions so producing two signals,  
 3 namely "pulse\_h" and "pulse\_l". The "pulse\_h" and  
 4 "pulse\_l" signals can then be used with a simple  
 5 modification to Arm C 132 so as to accommodate the  
 6 additional pulse selection via an additional selection  
 7 element ("and" or "mux") that selects the signal pulse'  
 8 129 origin as being for a high (pulse\_h) or low (pulse\_l)  
 9 data sequence. Additional clock phases would then be  
 10 required in order to separately control the rising and  
 11 falling edges of this additional selection of data  
 12 dependant sub pulses.

13

14 Figure 11 more clearly shows the signal timing and  
 15 logical relationships within the signal processing  
 16 apparatus of Figure 10 and illustrates the scheme from  
 17 the serial input signal "in" 1 to the electronic signal  
 18 ewave 25.

19

20 Using the above signal processing scheme a time-domain or  
 21 z-transform filter function is therefore effectively  
 22 synthesised where the energy of any bit is a function of  
 23 what has previously been sent. Expressing this in normal  
 24 z-domain sampled data convention.

25

$$26 \quad Y(z) = X(z) * H(z)$$

27

28 where:

29         $Y(z)$  is the relative energy of the output  
 30 sample

31         $X(z)$  is the relative energy of the input sample

32         $H(z)$  is the filter transfer function

33

$$34 \quad H(z) = A(1 - Bz^{-1})$$

1  
2 where:

3            A     =  $(T_s - dT_f - dT_r)$   
 4            B     =  $1 / (T_s + dT_f + dT_r - dT_l)$  for transmitted zeros  
 5        or  
 6            =  $1 / (T_s - dT_f - dT_r - dT_h)$  for transmitted ones

8 and where:

```
9      Ts= symbol bit period
10     dtl = pulse inversion period for
11           transmitted zeros
12     dTh = pulse inversion period for
13           transmitted ones
14     (as defined in Figure 9)
```

16 It should be noted that this z-domain technique does not  
17 completely describe the action of the filter invention as  
18 it does not describe how energy can be shifted within one  
19 sample.

20  
21 The described method and apparatus effectively provides a  
22 non linear (signal dependant) 1<sup>st</sup> order high frequency  
23 bandpass filter. By employing additional previous and  
24 future sample information through the incorporation of  
25 additional "latch" elements, and by using additional  
26 "xor" logical elements or similar structures, higher  
27 order high frequency band pass filters can readily be  
28 achieved.

29  
30 It will be obvious to one skilled in the art that by  
31 altering the timing of the various clock pulses the  
32 adaptable signal processor can be converted so as to act  
33 as a low frequency bandpass filter, the of order of which

1 is dictated by the number of "latch", or similar  
2 elements, incorporated within the circuit.

3

4 The apparatus if Figure 8 and 10 the signal processor  
5 uses no filter function to determine the  $S(n+1)''$   
6 signal. However, this can readily be made data dependant  
7 and filters can be readily implemented by using a variety  
8 of logical schemes such as used to generate the pulse  
9 121.

10

11 Furthermore the apparatus of Figure 8 and 10 suggests  
12 that the signals are single bit digital lines. In  
13 practice they would most likely be differential signals  
14 with differential source coupled logic cells. These  
15 figures also suggest that the signals are only one bit  
16 wide but similar architecture using multiple bit wide  
17 parallel data lines could be used in high bandwidth  
18 systems with time-interleaving appropriately used for  
19 improved power trade-offs.

20

21 Aspects of the present invention described herein refer  
22 to a single channel communications system. However, in  
23 alternative embodiments, more channels can be employed,  
24 such as in a multi-core optical fibre or multi-strand  
25 twisted-pair e.g. CAT-5 cabling. The described aspects  
26 also refer to a communication system with a single  
27 channel with a single transmission signal present on the  
28 channel. However, in some embodiments, transmissions can  
29 be across one or more shared media channels using one or  
30 more signals such as, but not limited to, optical wave  
31 division multiplexing schemes (DWDM, CWDM), using  
32 multiple equalisers per signal.

33

1 The preferred embodiment of the present invention  
2 describes use mainly within the context of a fibre optic  
3 medium, however it is anticipated that it may be employed  
4 with alternative transmission medium including, but not  
5 limited to, over air, optical fibre, printed circuit  
6 board or cable. Similarly aspects of the present  
7 invention may employ alternative transmission signal  
8 formats including, but not limited to, modulated, un-  
9 modulated, return to zero coding, non return to zero  
10 coding, encoded data, non encoded data, multi-level,  
11 binary, continuous or discontinuous, framed, burst or  
12 packet based or any combination of these. Furthermore,  
13 aspects of the present invention may employ alternative  
14 transmission technique including, but not limited to,  
15 electrical, electro-magnetic, magnetic or optical means.

16

17 The apparatus of aspects of the present invention present  
18 the transmitter 2 and the receiver 4 as two separate  
19 elements or components. Alternative embodiments that  
20 comprise multiple channel and bi-directional systems that  
21 incorporate transmitters and receiver that are joined or  
22 part joined within the same combined element or component  
23 of the system with the equaliser possibly additionally  
24 contained within.

25

26 The described apparatus further describes that the  
27 transmitter 2 is a distinct and separate element made up  
28 of two parts, the adaptable equaliser 7 and the optical  
29 source 8. However, alternative embodiments are envisaged  
30 where the transmitter element may also include a  
31 combination of additional separate, not necessarily  
32 distinct elements in any combination or form, such as a  
33 parallel to serial data converter, clock-data recovery

1 unit, re-synchroniser, line driver, equaliser, optical  
2 source driver and the optical source itself.

3

4 Further alternative embodiments of aspects of the present  
5 invention include the communications system containing  
6 additional filters, transducers, amplifiers, sensors or  
7 other elements or components between multiple or single  
8 transmitters, receivers and medias. In addition the  
9 communication system could contain continuous or separate  
10 sections of media, separated by filters, transducers,  
11 sensors, transponders, transceivers, transmitters,  
12 receivers or other elements so as to break the media into  
13 one or more sections of not necessarily the same type of  
14 media.

15

16 The input signal 1, synthesis electronic signal ewave 25,  
17 optical wave owave 26 and apparatus presents a solution  
18 to a single binary on-off coding scheme. However, the  
19 principle can be applied to similar waves that are  
20 encoded in multiple levels such as a pulse amplitude  
21 modulation scheme (PAM encoding) and signal processing  
22 provided using a similar method.

23

24 In systems where the output amplitude can also be also  
25 directly influenced by the instantaneous amplitude of the  
26 ewave signal 25, additional equalisation can be applied  
27 using an amplitude modulation technique or the  
28 superposition of an additional pulse onto the ewave  
29 signal as appropriate to increase the energy of the  
30 signal in the frequencies of interest. A superposition  
31 technique such as analogue summation could be used.

32

33 Described herein is a method and apparatus for adapting  
34 an information carrying signal within of before an

1 associated transmitter. This adaptation provides an  
2 efficient way of not only producing frequency dependent  
3 filters but also provides an effective means for the  
4 equalisation of the information carrying signal. The  
5 transmitter effectively equalises by providing a pre-  
6 correction or compensation of the signal. As a result  
7 the transmitter based equalisation schemes described is  
8 capable of achieve higher performance than other prior  
9 art systems where equalisation takes place within the  
10 receiver or elsewhere in the channel. This effect is a  
11 direct result of the fact that this system can be  
12 designed so that the desired information carrying signal  
13 can be kept above the noise or other interference levels  
14 and hence can be more easily interpreted at the receiver.  
15 Furthermore, as the transmitter has an intrinsically  
16 accurate knowledge of what it is trying to transmit, and  
17 given information on what signal impairments exist in the  
18 system, more simplistic, intelligent, signal aware  
19 schemes such as those described above are possible.

20

21 A significant advantage of the described system is that  
22 it is very accurately controllable, has a fine  
23 resolution, a wide equalisation range, requires few high  
24 performance circuit elements to implement, requires less  
25 components or circuitry, requires little additional power  
26 and can be designed for low cost and high volume  
27 manufacturing than existing known schemes.

28

29 Additionally, because the synthesis technique is more  
30 controllable, this invention can provide more  
31 sophisticated equalisation or compensation for affects  
32 other simple bandwidth limitations such as complex non-  
33 linear and signal dependant ones. One practical use of  
34 this scheme is in high-speed fibre-optic systems where

1 transmission distances are greatest and channel  
2 impairments are complex. Examples of such complex  
3 impairments include modal, chromatic and polarisation  
4 dispersion and chirp of the optical fibre, saturation and  
5 scattering properties of the optical source and  
6 asymmetries and bandwidth limitations of the optical  
7 transmitter and receiver responses.

8

9 A further advantage of aspects of the present invention  
10 is that because both the eye closure 29 per length of  
11 media is improved and because the data jitter 28 per unit  
12 media is reduced, greater distance can be travelled  
13 before complete opto-electronic-opto signal regeneration  
14 or re-timing units are required. This greatly benefits  
15 the systems because it enables cheaper all optical  
16 systems to be made.

17

18 A yet further advantage is that more cost effective,  
19 lossy or dispersive media can be used and over greater  
20 distances in higher data rate applications. For example,  
21 twisted pair could be used where previously coaxial cable  
22 would have been required or multi-mode fibre where  
23 previously single-mode fibre was used.

24

25 Generally the method and apparatus of aspects of the  
26 present invention provide for the development and  
27 manufacture of higher performance communications systems,  
28 including optical ones, that are less expensive, less  
29 complex, less power demanding or more compact.

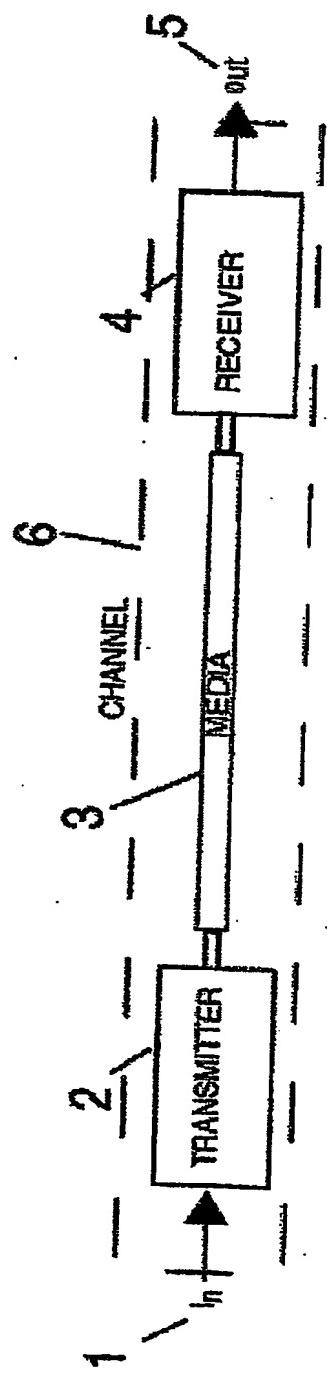
30

31 The foregoing description of the invention has been  
32 presented for purposes of illustration and description  
33 and is not intended to be exhaustive or to limit the  
34 invention to the precise form disclosed. The described

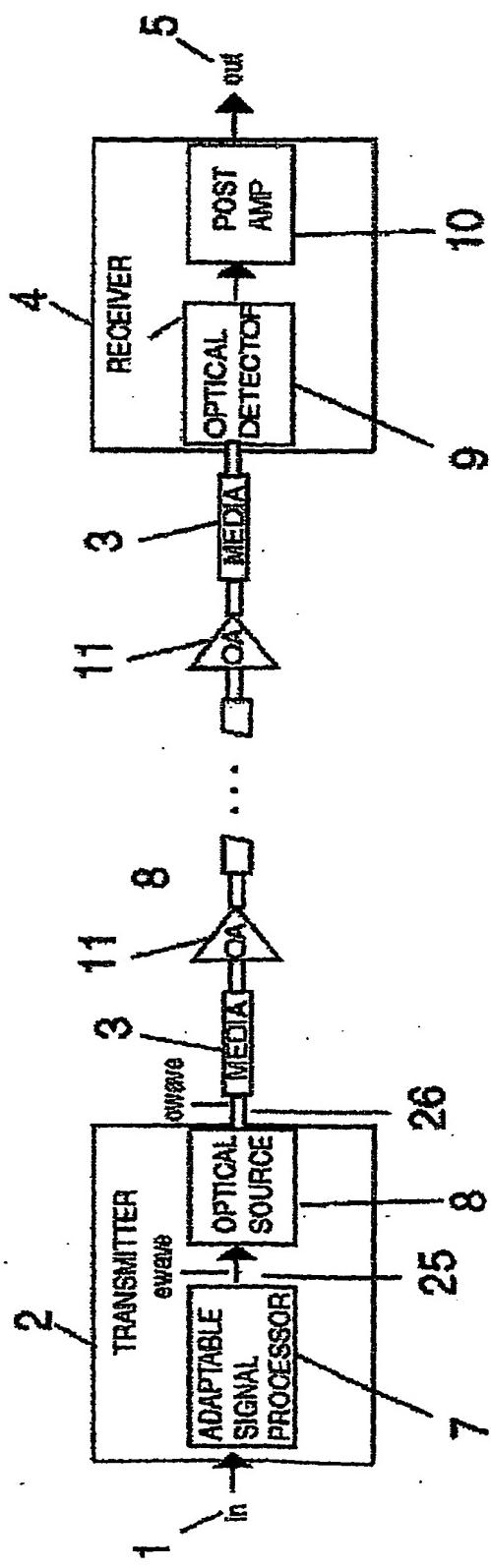
1 embodiments were chosen and described in order to best  
2 explain the principles of the invention and its practical  
3 application to thereby enable others skilled in the art  
4 to best utilise the invention in various embodiments and  
5 with various modifications as are suited to the  
6 particular use contemplated. Therefore, further  
7 modifications or improvements may be incorporated without  
8 departing from the scope of the invention herein  
9 intended.

1/9

Figure 1



2/9  
Figure 2



3/9

Figure 3

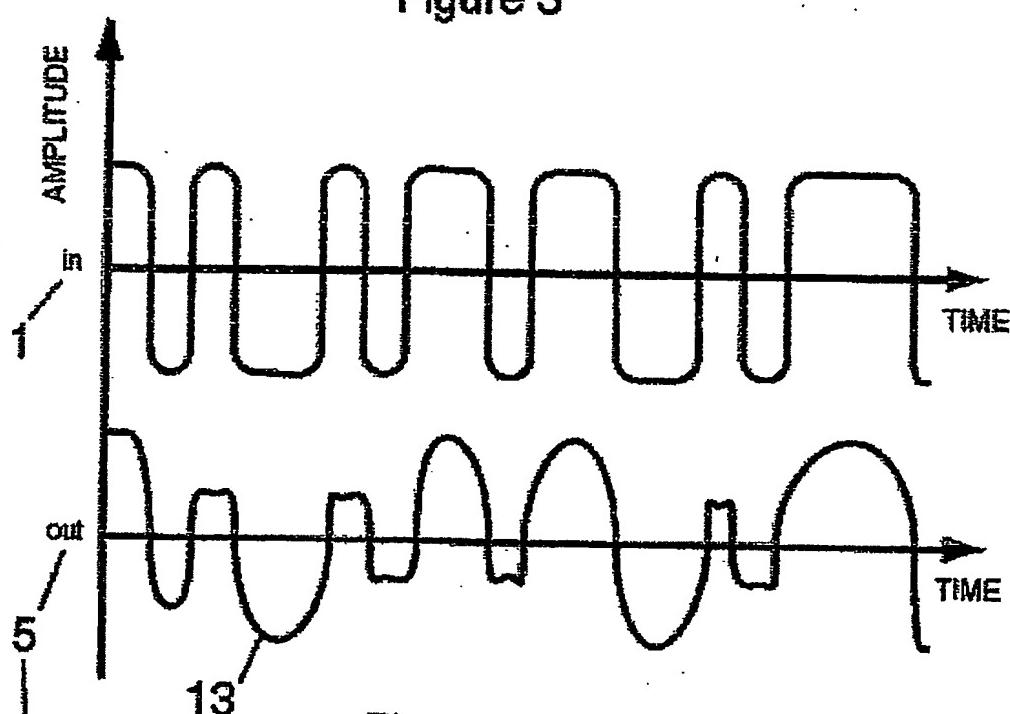


Figure 4

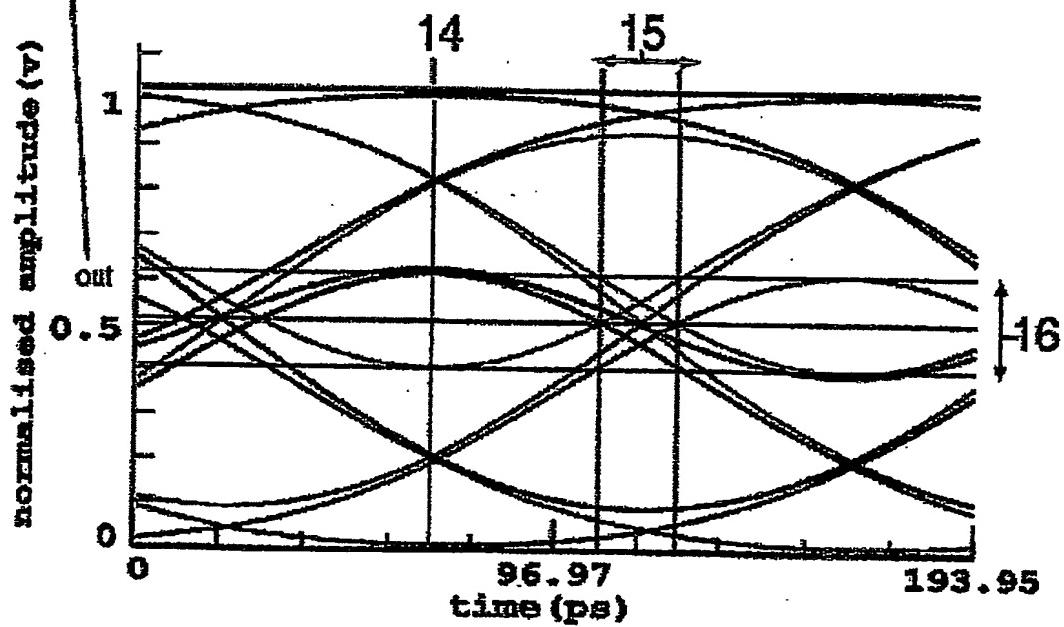
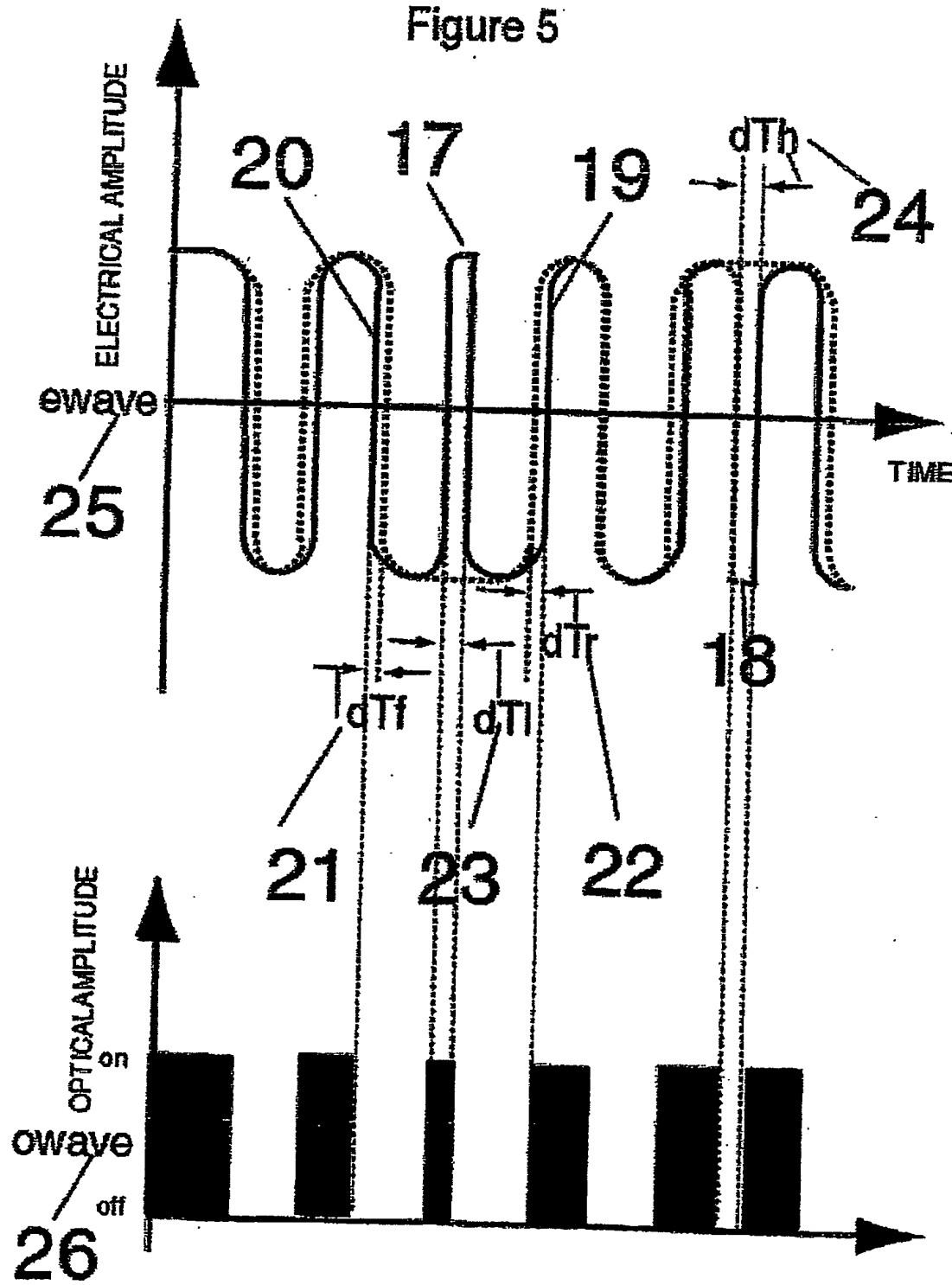


Figure 5



5/9

Figure 6

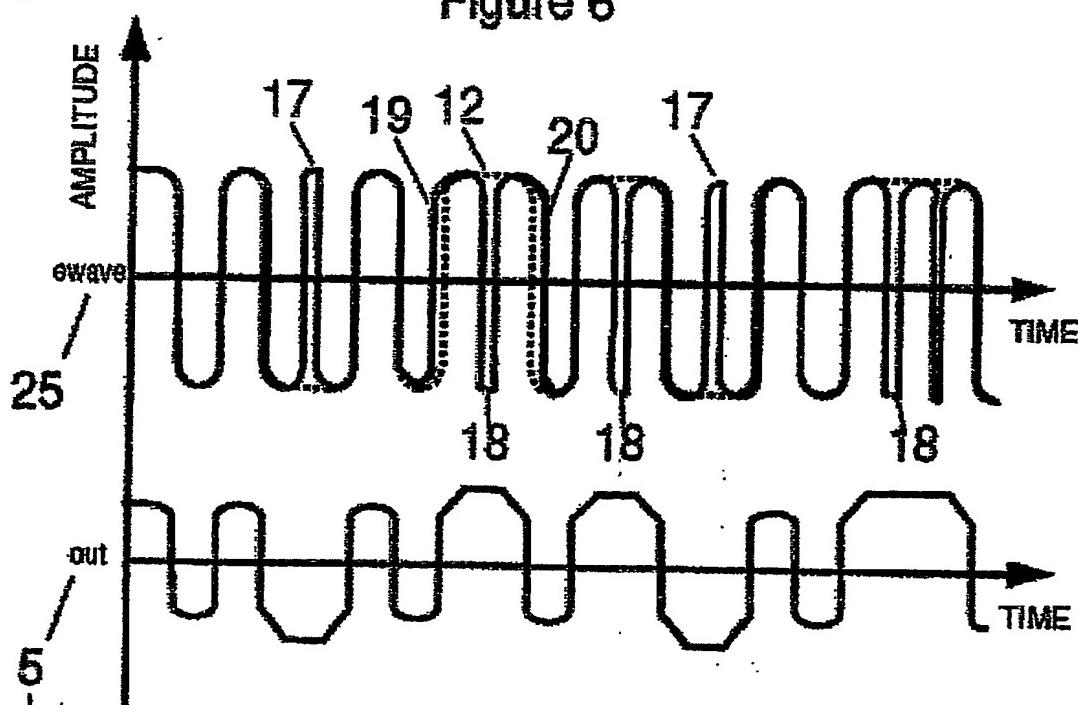


Figure 7

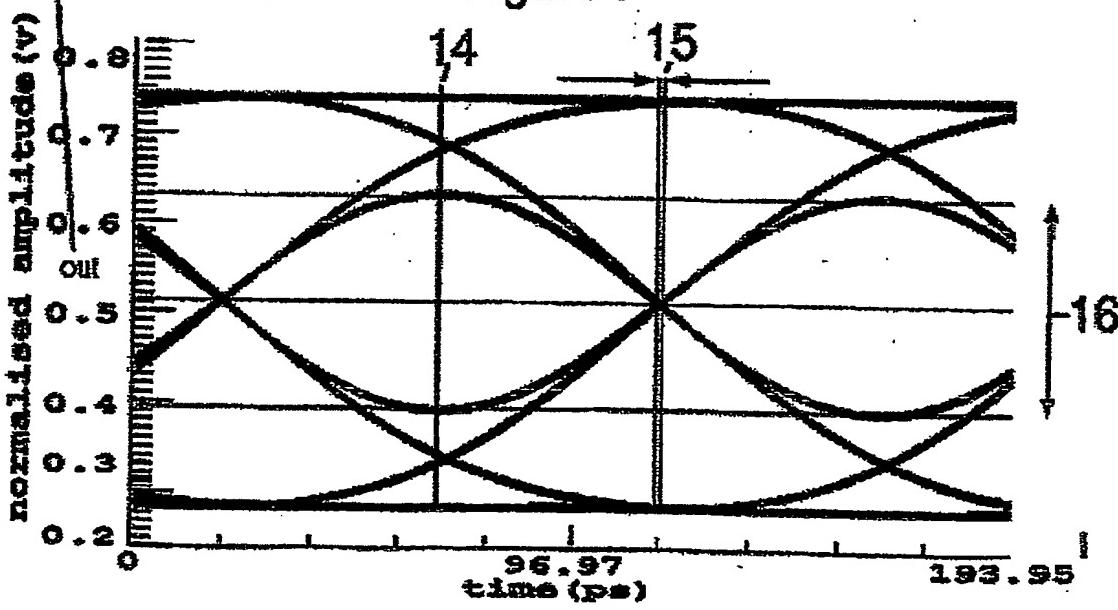
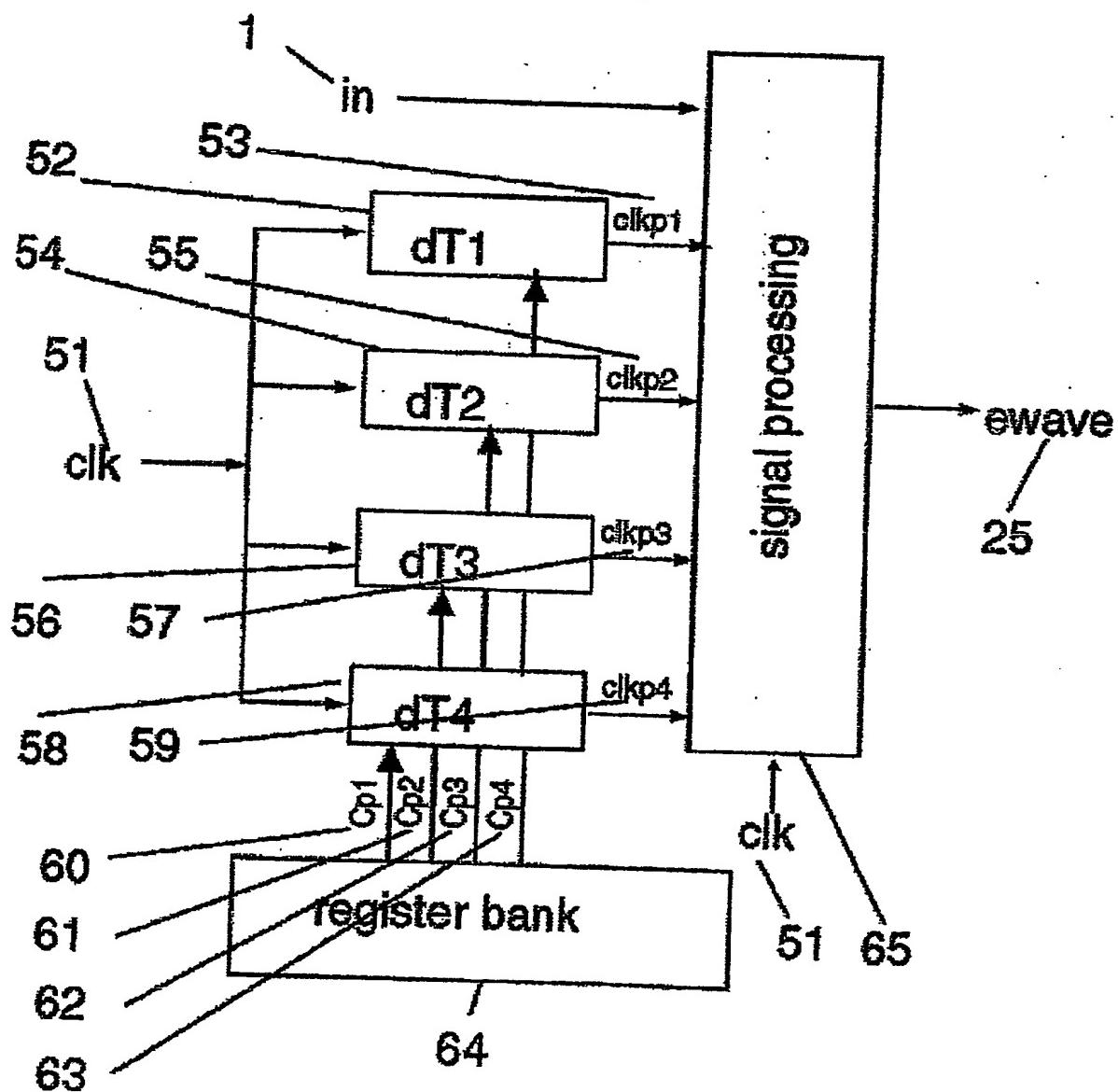


Figure 8



7/9  
Figure 9

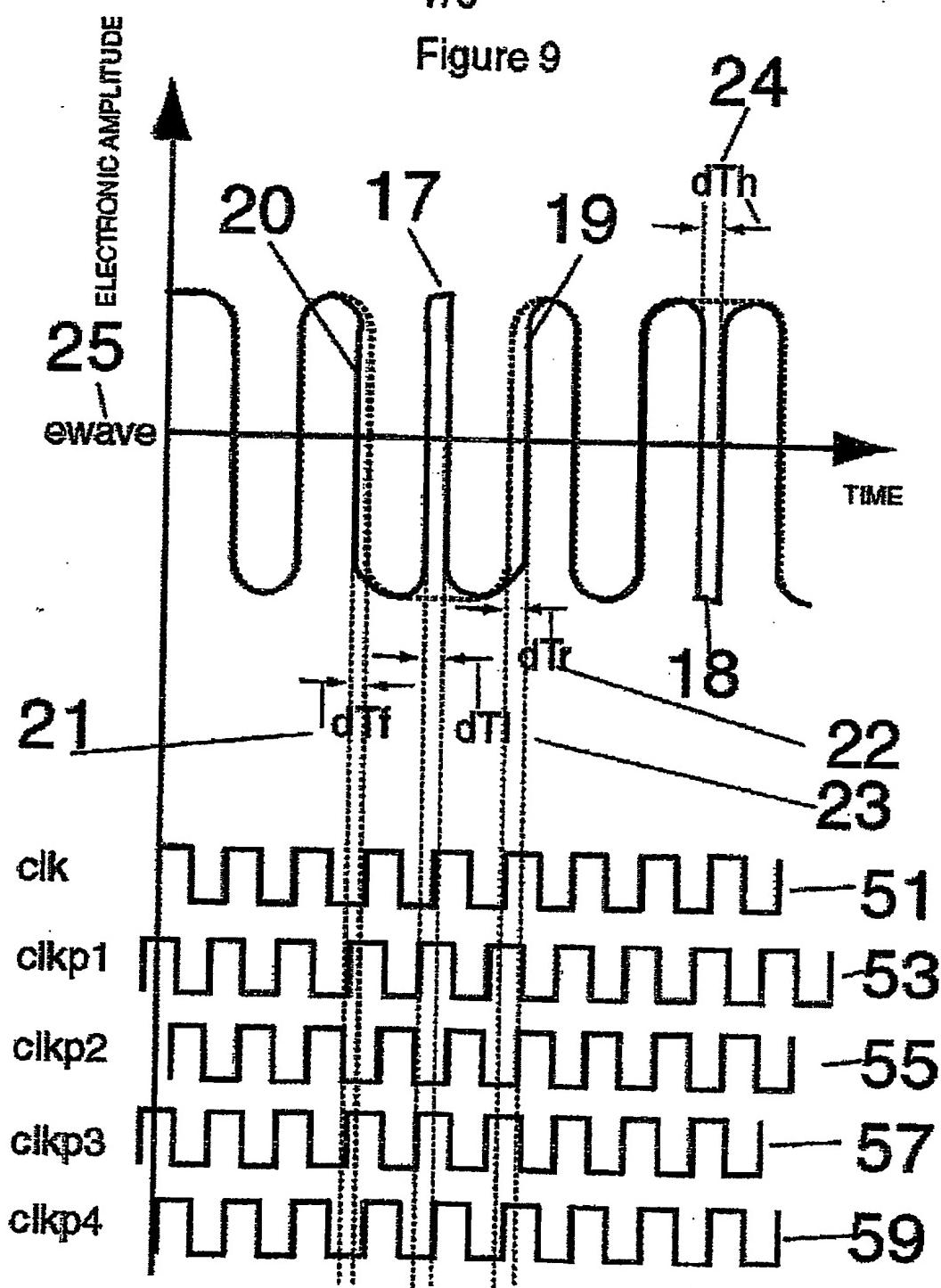
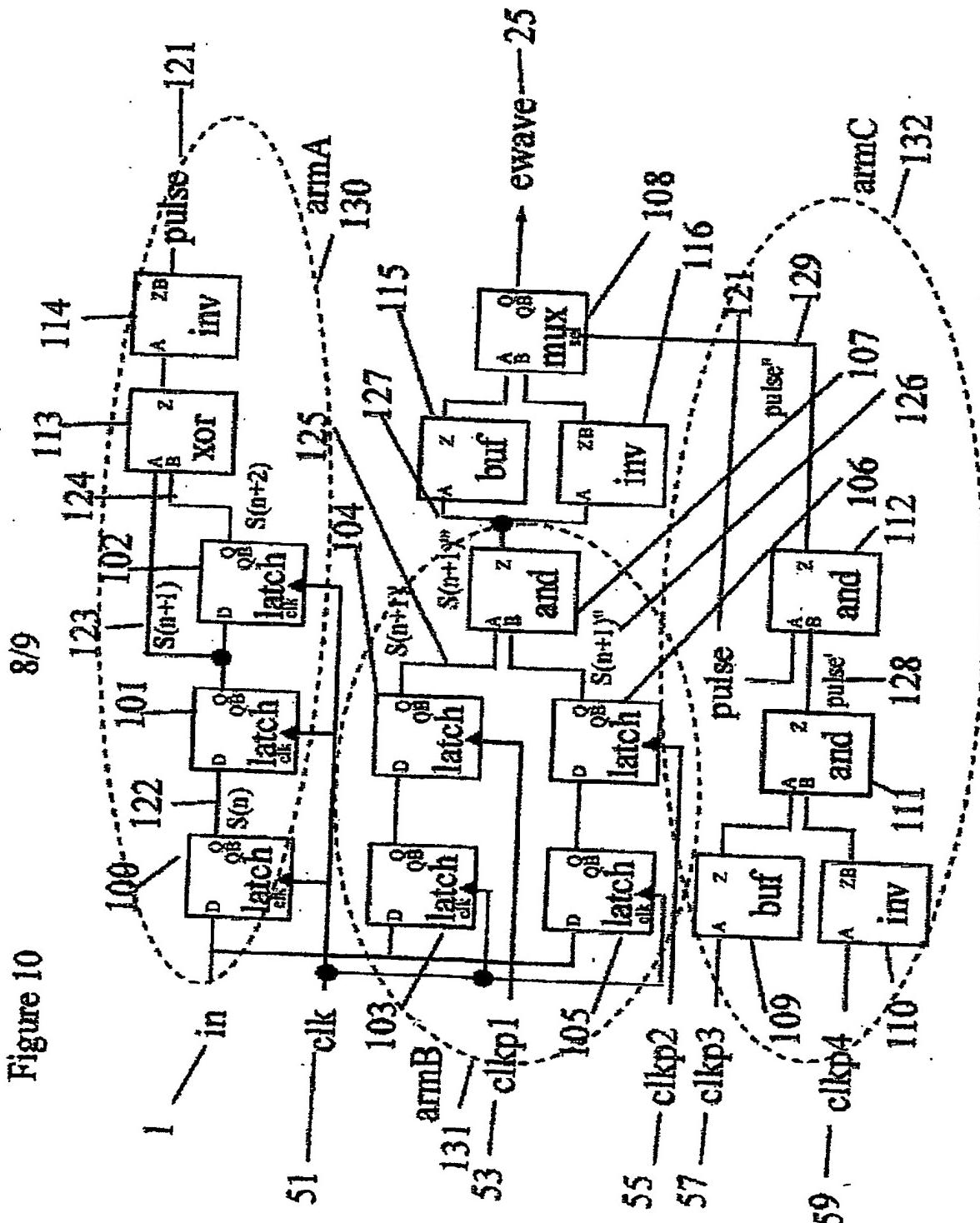
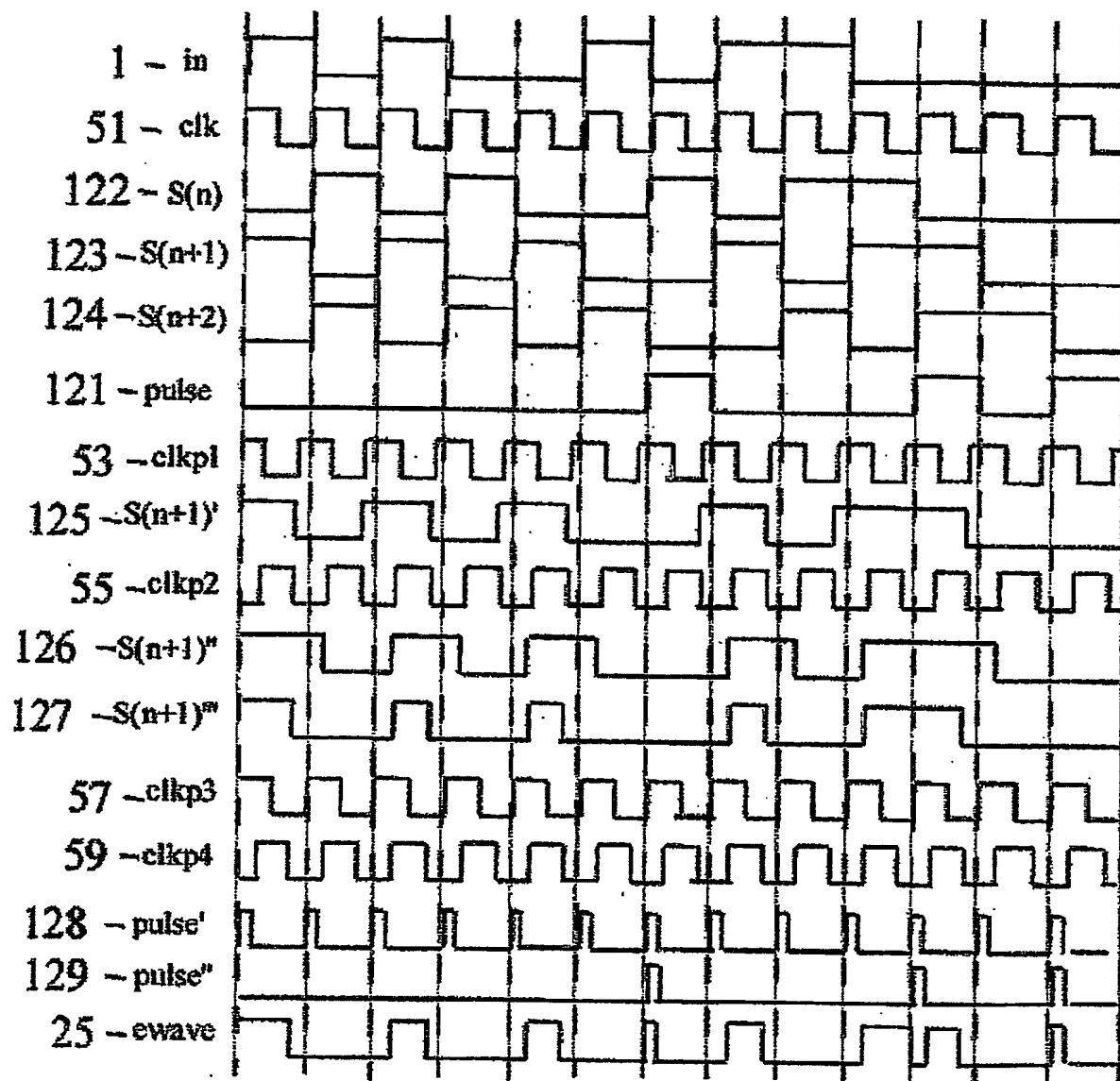


Figure 10



9/9

Figure 11



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